WHAT IS CLAIMED IS:

1. A semiconductor circuit comprising:

a MOS transistor having:

spaced-apart source and drain regions of a first conductivity type that contact a semiconductor region of a second conductivity type, the semiconductor region having a top surface, one of the source and drain regions having a first bottom point that lies furthest away from the top surface, and a first depth measured from the top surface to the first bottom point along a line perpendicular to the top surface;

a channel region located between the source and drain regions; and

a gate formed over, and insulated from, the channel region; and

an imaging cell having:

spaced-apart source and drain regions of the first conductivity type that contact the semiconductor region, one of the source and drain regions of the imaging cell having a second bottom point that lies furthest away from the top surface, and a second depth measured from the top surface to the second bottom point along a line perpendicular to the top surface;

a channel region located between the source and drain regions of the imaging cell; and

a floating gate formed over, and insulated from, the channel region of the imaging cell.

2. The semiconductor circuit of claim 1 wherein the second depth is substantially larger than the first depth.

3. The semiconductor circuit of claim 2 and further comprising a control gate well of the first conductivity type, the floating gate being formed over, and insulated from, the control gate well.

4. The semiconductor circuit of claim 2 and further comprising a layer of oxide formed on the channel region of the imaging circuit and the control gate well, and under the floating gate.

5. The semiconductor circuit of claim 4 wherein the layer of oxide has a thickness that retains electrons for a period of time greater than six months.

6. The semiconductor circuit of claim 1 and further comprising a layer of oxide formed on the channel region of the imaging circuit and the control gate well, and under the floating gate, the layer of oxide having a thickness that retains electrons for a period of time that is greater than zero and less than three seconds.

7. The semiconductor circuit of claim 6 wherein the control gate well is formed in the semiconductor material.

8. The semiconductor circuit of claim 6 and further comprising an intermediate well that contacts the semiconductor material, the control gate well contacting the intermediate well, the intermediate well having an opposite conductivity type as the control gate well and the semiconductor material.

9. The semiconductor circuit of claim 2 wherein the control gate well contacts the semiconductor material.

10. The semiconductor circuit of claim 2 and further comprising an intermediate well that contacts the semiconductor material, the control gate well contacting the intermediate well, the intermediate well having an opposite conductivity type as the control gate well and the semiconductor material.

11. The semiconductor circuit of claim 2 and further comprising a control gate formed over, and insulated from, the floating gate.

12. A method of operating an imaging cell, the imaging cell having:

spaced-apart source and drain regions of the first conductivity type that contact a semiconductor region of a second conductivity type;

a channel region located between the source and drain regions; and

a floating gate formed over, and insulated from, the channel region,

the method comprising the steps of:

erasing the floating gate by removing a plurality of charge carriers from the floating gate; and

reading the imaging cell to determine an initial integration current by measuring a current that flows between the source and drain regions.

13. The method of claim 12 and further comprising the step of exposing the channel region to light energy for a predetermined period of time.

14. The method of claim 13 and further comprising the step of reading the imaging cell to determine a final integration current by measuring a current that flows between the source and drain regions after the predetermined period of time has expired.

15. The method of claim 14 and further comprising the step of subtracting the final integration current from the initial integration current.

16. The method of claim 13 wherein the imaging cell further includes a well of the first conductivity type, the floating gate being formed over, and insulated from, the well.

17. The method of claim 16 wherein the plurality of charge carriers are removed from the floating gate by grounding the source region, the drain region, and the semiconductor region, and placing a positive potential on the well.

18. The method of claim 16 wherein ground is placed on the well when the channel region is exposed to light energy.

19. The method of claim 13 wherein the imaging cell further includes a control gate that is formed over, and insulated from, the floating gate.

20. The method of claim 14 wherein the imaging cell is read to determine an initial integration current after the imaging cell has been read to determine a final integration current.